REMARKS

By way of the present response, claims 1, 2, 10, 12, 17 and 19 are amended. Claims 1-20 currently are pending. In view of the above amendments and the remarks advanced below, reconsideration and withdrawal of the rejections of the claims is respectfully requested.

Page 2 of the action includes a rejection of claims 1-20 under 35 U.S.C. 112, second paragraph, as allegedly being indefinite. In the rejection, the Examiner asserts that the claim language, "the second circuit area includes a circuit, which is subject to noise," is unclear. While it is believed one of ordinary skill in the art would understand the meaning of this phrase, as recited in the claims, especially when read in light of the specification, independent claims 1, 2 and 10 have been changed. The independent claims now recite, among other things, the feature of a circuit susceptible to influence of noise from outside the circuit.

Support for the amendments is found throughout Applicants' original disclosure, for instance, in the exemplary embodiment shown in Figures 1 and 2, and the description thereof starting at line 23 of page 4 of the specification. As described therein, a semiconductor chip includes an area or region in which circuit elements susceptible to influence of noise are arranged (e.g., see the paragraph spanning pages 8 to 9). It is respectfully submitted that the amended claims are clear, especially when considering the problems of reduced circuit element reliability caused by noise generated by elements outside the circuit element (e.g., wiring), as described in connection with the related art (see, page 2, lines 3-18). For at least these reasons, it is believed the rejection under Section 112, second paragraph, should be withdrawn.

Claims 1-20 are rejected under 35 U.S.C. § 102(e) as being anticipated by Kawaishi (U.S. Patent No. 6,798,071). However, Applicants respectfully submit that each of amended independent claims 1, 2 and 10 recite subject matter not described in the Kawaishi patent. For instance, Kawaishi does not describe, using any reasonable interpretation of the claim language, the combinations of features including *inter alia* "the first semiconductor chip has ... a second circuit area which is positioned between the first electrode group and the second electrode group, and wherein the second circuit area includes a circuit which is susceptible to

influence of noise caused outside the circuit," as recited in independent claim 1, "a first semiconductor chip having a first circuit element region and a second circuit element region which is apart from the first circuit element region ..., wherein the second circuit element region includes a circuit which is susceptible to influence of noise caused outside the circuit," as recited in claim 2, and "a first semiconductor chip having a first circuit area, a second circuit area surrounding the first circuit area ..., wherein the second circuit area includes a circuit which is susceptible to influence of noise caused outside the circuit," as set forth in independent claim 10.

With reference to Figures 3 and 6 and column 6 of, the Examiner asserts that the relay electrodes of the Kawaishi patent are circuits. It is respectfully submitted, however, that the relay electrodes of Kawaishi, which merely comprise a plurality of connected wires (e.g., metal wires 31, 32 and 33), are not circuits. That is, those of ordinary skill in the art would readily appreciate that a circuit as recited in the context of Applicants' claims and as described in disclosure would comprise a set of electronic components, for example, a transistor, a resistor, capacitor etc., which are connected with each other through wiring to perform a particular function in an electronic system. In contrast, the metal wire 31 located between the metal wire 32 and the metal wire 33 constituting a relay electrode in the Kawaishi patent would transfer whatever voltage or signal that is present on the lead frame to an upper chip electrode. Kawaishi does not otherwise disclose or imply that a circuit is located between the metal wire 32 and the metal wire 33, much less a circuit susceptible to influence of noise caused outside the circuit. For at least these reasons, the Kawaishi patent fails to describe, within any reasonable interpretation, each and every claimed feature recited in the context of independent claims 1, 2 and 10. Accordingly, the rejection should be withdrawn.

The remaining claims depend from one of independent claims 1, 2 and 10, and therefore are considered allowable at least for the above reasons, and further for the additional features recited.

Based on the foregoing, the present application is now believed to be in condition for allowance. Prompt notification of the same is earnestly solicited.

Respectfully submitted,

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